

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel A. Day

Title: Selective Control of Test-Access Ports in Integrated Circuits

Docket No.: 884.879US1

Filed: June 30, 2003

Examiner: Unknown



Serial No.: 10/612293

Due Date: N/A

Group Art Unit: 2857

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

☒ A return postcard.

☒ An Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 8 cited documents.

If not provided in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

By: 

Atty: Eduardo E. Drake

Reg. No. 40,594

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20 day of April, 2004.

Name

KACIA LEE

Signature

Kacia Lee

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

S/N 10/612293

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Daniel A. Day	Examiner:	Unknown
Serial No.:	10/612293	Group Art Unit:	2857
Filed:	June 30, 2003	Docket:	884.879US1
Title:	Selective Control of Test-Access Ports in Integrated Circuits		
Assignee:	Intel Corporation	Customer No:	21186

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

Serial No : 10/612293

Filing Date: June 30, 2003

Title: Selective Control of Test-Access Ports in Integrated Circuits

Assignee: Intel Corporation

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The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

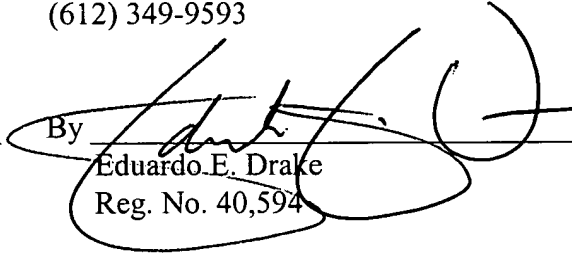
DANIEL A. DAY

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Name

KACIA LEE

Signature

Kacia Lee

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <small>(Use as many sheets as necessary)</small>	Complete if Known <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Application Number</td> <td>10/612293</td> </tr> <tr> <td>Filing Date</td> <td>June 30, 2003</td> </tr> <tr> <td>First Named Inventor</td> <td>Day, Daniel</td> </tr> <tr> <td>Group Art Unit</td> <td>2857</td> </tr> <tr> <td>Examiner Name</td> <td>Unknown</td> </tr> </table>	Application Number	10/612293	Filing Date	June 30, 2003	First Named Inventor	Day, Daniel	Group Art Unit	2857	Examiner Name	Unknown
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Group Art Unit	2857										
Examiner Name	Unknown										
Sheet 1 of 1	Attorney Docket No: 884.879US1										



US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-5,396,501	03/07/1995	Sengoku, Shoichiro	371	22	09/30/1992
	US-6,122,762	09/19/2000	Kim, Ho-Ryong	714	726	09/15/1998
	US-6,446,230	09/03/2002	Chung, Sung S.	714	726	09/14/1998
	US-6,449,755	09/10/2002	Beausang, James , et al.	716	5	07/14/2000

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"Boundary Scan (JTAG) Tools and Circuit Board Test Solutions", www.acculogic.com/Products/BoundaryScanHome.htm , 2 pages	
		"Designing for On-Board Programming Using the IEEE 1149.1 (JTAG) Access Port", Intel AP-630 Application Note, Intel order no. 292186-002, available from http://www.intel.com , (November 1996), 14 pages	
		"Joint Test Action Group from FOLDOC", Available from http://wombat.doc.ic.ac.uk/foldoc/foldoc.cgi?Joint+Test+Action+Group , (11/15/1999), 1 page	
		"The New Vanguard 330 From Integrated Measurement Systems Offers Cost-Effective Validation of High Performance Logic ICs", www.engineering-uk.co.uk , (04/24/2001), 2 Pages	

EXAMINER

DATE CONSIDERED